AMENDMENTS TO THE CLAIMS:

Listing of claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Claim 1 (Currently Amended): A logic circuit, comprising:

a first inversion section for inverting a first input signal having a first logic level and outputting an inverted first input signal;

a second inversion section for inverting a second input signal having a logic level opposite the first logic level, and outputting an inverted second input signal; and

a transmission section for ~~selecting between~~ receiving the inverted first input signal and the inverted second input signal and outputting one of the inverted first input signal and the inverted second input signal,

wherein the ~~inverted first input signal of said first inversion section and the inverted second input signal of said second inversion section in response to~~ transmission section comprises electrically connected transistors that respectively receive the inverted first input signal and the inverted second input signal, and the connected transistors output one of the inverted first input signal and the inverted second input signal in response to an externally controllable selection signal and an inverted signal of the selection signal.

Claim 2 (Currently amended): A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting ~~the~~ an inverted first input signal;

a second inversion section for inverting a second input signal and outputting ~~the~~ an inverted second input signal;

a first outputting section comprising electrically connected transistors for ~~selecting between outputting~~ respectively receiving the inverted first input signal and the inverted second input signal, and the electrically connected transistors output one of the ~~output of said first inversion section and the output of said second inversion section~~ inverted first input signal and the inverted second output signal in response to an externally controllable first selection signal and an inverted signal of the first selection signal; and

a second outputting section comprising electrically connected transistors for ~~selecting between outputting~~ respectively receiving the inverted first input signal and the inverted second input signal, and the electrically connected transistors output one of the ~~output of said first inversion section and the output of said second inversion section~~ inverted first input signal and the inverted second input signal in response to an externally controllable second selection signal and an inverted signal of the second selection signal.

Claims 3-6 (canceled)

Claim 7 (Previously Presented): A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting the inverted signal of the first input signal and outputting a resulting signal;

a first outputting section for performing NANDing arithmetic between the output of said first inversion section and a second input signal and outputting a first resulting signal; and

a second outputting section for performing NANDing arithmetic between the output of said second inversion section and an inverted signal of the second input signal and outputting a second resulting signal;

said first outputting section and said second outputting section being switched with the second input signal and the inverted signal of the second input signal, said first outputting section outputs the first resulting signal and said second outputting section outputs the second resulting signal.

Claim 8 (Currently Amended): The logic circuit as claimed in claim 1, further comprising:

a first switching section provided on an input side of said first inversion section and ~~capable of~~ performing switching of whether the first input signal ~~should be~~ is passed to the first inversion section or blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and ~~capable of~~ performing switching of whether the second input signal ~~should be~~ is passed to the second inversion section or blocked in accordance with the external control signal.

Claims 9-12 (canceled)

Claim 13 (Currently Amended): A logic circuit, comprising:

a first inversion section for inverting a first input signal having ~~one of~~ positive logic and negative logic and outputting an inverted first input signal, said first inversion section including transistor circuits, each of said transistor circuits having a first input signal terminal for inputting the first input signal~~, a first input selection signal terminal for a controllable selection signal~~ and an outputting terminal for outputting ~~the selection signal or~~ the inverted signal based on the logic of the first input signal;

a second inversion section for inverting a second input signal having negative logic and positive logic, said second inversion section including transistor circuits, each of said transistor circuits having a second input signal terminal for inputting the second input signal~~, a second input selection signal terminal for the controllable selection signal~~ and an outputting terminal for outputting ~~the selection signal or~~ the inverted signal based on the logic of the ~~first~~ second input signal; and

a transmission section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable selection signal and an inverted signal of the selection signal, said transmission selection including transistor circuits, each of said transistor circuits having a first selection signal terminal for inputting the controllable selection signal and a second selection signal terminal for inputting the inverted signal of the selection signal.

Claim 14 (canceled)

Claim 15 (Currently Amended): A logic circuit, comprising:

a first inverter inverting a first input signal having a first logic level and outputting an inverted first input signal;

a second inverter inverting a second input signal having a logic level opposite the first logic level and outputting an inverted second input signal; and

a selector to receive the inverted first input signal and the inverted second input signal and to selectively output one of the inverted first input signal and the inverted second input signal,

wherein the selector ~~receives~~ comprises electrically connected transistors that respectively receive the inverted first input signal and the inverted second input signal, and the connected transistors output one of the inverted first input signal and the inverted second input signal in response to an externally controllable selection signal and an inverted signal of the selection signal ~~and selects the inverted first input signal in response to the externally controllable selection signal and the inverted signal being in one logic state and selects the inverted second input signal in response to the selection signal and the inverted signal being in another logic state~~.

Claim 16 (New): A logic circuit, comprising:

a first inversion section for inverting a first input signal positive logic and negative logic and outputting an inverted first input signal, said first inversion section including CMOS logic circuits, each of said CMOS logic circuits having a first input signal terminal for inputting the first input signal, and an outputting terminal for outputting the inverted signal based on the logic of the first input signal;

a second inversion section for inverting a second input signal having negative logic and positive logic, said second inversion section including CMOS logic circuits, each of said CMOS logic circuits having a second input signal terminal for inputting the second input signal and an outputting terminal for outputting the inverted signal based on the logic of the second input signal; and

a transmission section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable section signal and an inverted signal of the selection signal, said transmission section including CMOS logic circuits, each of said CMOS logic circuits having a first selection signal terminal for inputting the controllable selection signal and a second selection signal terminal for inputting the inverted signal of the selection signal.